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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1

of 2

Completeness if Known

Application Number	10/603,579
Filing Date	June 25, 2003
First Named Inventor	Franck Badets, et al.
Art Unit	2651 2B16
Examiner Name	Not yet assigned Lam, T
Attorney Docket Number	STM07-02021

U. S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ²
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
W	AD	EP 0 326 202	08/02/1989	Catena		
W	AE	WO 00/65717	11/02/2000	Seiko Epson Corp (JP)	(Abstract only)	

Examiner
Signature

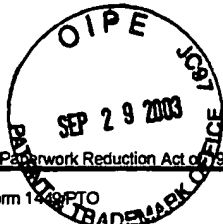
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PTO/SB/08B (08-03)

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Complete if Known

Application Number	10/603,579
Filing Date	June 25, 2003
First Named Inventor	Franck Badets, et al.
Art Unit	2631 2816
Examiner Name	Not yet assigned Lam, T
Attorney Docket Number	STMI07-02021

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
W	AF	RICHTER, R., et al. "A VIRTUAL CLOCK ENHANCEMENT METHOD FOR DDS USING AN ANALOG DELAY LINE"; IEEE Journal of Solid state Circuits, Vol. 36, No. 7, July 2001; pages 1158-1161;	
W	AG	NOSAKA, H., et al.; "A LOW-POWER DIRECT DIGITAL SYNTHESIZER USING A SELF-ADJUSTING PHASE-INTERPOLATION TECHNIQUE"; IEEE Journal of Solid-State Circuits, Vol. 36, No. 8, August 2001; pages 1281-1285;	
W	AH	Chapitre 3; Oscillateurs Synchrones; pages 99-126	

Examiner Signature		Date Considered	9/17/2004
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